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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,731	01/24/2002	Jim Janesick	01901071	3160

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,731	JANESICK, JIM	
	Examin r	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34 and 58-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34 and 58-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 10/16/03 has been entered.

Election/Restriction

2. In Paper #8 filed on 4/29/03, on page 7, applicant expressly admits that the inventions claimed in claims 1-34 and 58-71 are obvious over each other within the meaning of 35 USC § 103. In light of this admission, the requirement of an election of species has been withdrawn.

Drawings

3. The drawings remain objected to by the PTO Draftsperson for the reasons noted on the Notice of Draftsperson's Patent Drawing Review, form PTO-948 attached to the paper mailed 07/08/2003. The fact that the application has not been deemed abandoned does not implicitly withdraw the Draftsperson's objections.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

A. Claims 1-11,12-22,23-34,58-69,70, and 71 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Each of claims 1,12,23,58,70, and 71, as amended, recites a combination including "a substrate connected to a voltage," and which requires "the pinned transfer gate being connected to the voltage." Applicant thus claims a device having a voltage, said device being provided with the means to connect a substrate to said voltage, said device being further provided with the means to connect a pinned transfer gate to said voltage. Applicant's original application disclosed "The pinned transfer gate is "pinned" because the p++ doped pinned region 219 is tied (or "pinned") to the potential of the substrate 202, typically ground or zero volts," Application, page 7, lines 6 and 7, and "The pinned aperture region 304 (like the pinned transfer gate 206) is tied to the substrate 202 potential," Application, page 9, lines 24-25. Thus the application as filed disclosed a substrate which existed at a voltage (typically ground), a pinned transfer gate, and that the pinned transfer gate was tied to the voltage of the substrate. However, the application as filed did not disclose a voltage independent of the substrate, or the means to connect the substrate to that voltage, or the means to connect the pinned transfer gate to that voltage. Furthermore, the application as filed did not disclose any means whatsoever to

enable a connection between the substrate and the pinned transfer gate where such a connection was able to assure that the substrate and the pinned transfer gate were at the same potential. Applicant's claims will be examined under the assumption that applicant actually merely intended to claim that in the device claimed, the pinned transfer gate was connected to the substrate in such a way that the voltage of the pinned transfer gate was related to the voltage of the substrate.

B. Claims 1-34 and 58-71 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. These claims are directed to combinations that include an element referred to as a "Pinned Transfer Gate," that is connected to the voltage of a substrate. It is not known in the art how to make and use a "Pinned Transfer Gate," nor has Applicant sufficiently explained how to do so. In particular, Applicant has not shown, nor is it known to the art, how to tie connect the "Pinned Transfer Gate" to the voltage of the substrate.

In the context, not of an imager but rather of a charge transfer device, Hynecek 4,994,875 discloses a "virtual transfer gate" wherein a "virtual electrode" prevents electrons from transferring until the voltage on an insulated "conductive electrode" reaches a critical negative voltage. Hynecek's "virtual electrode" is a P type region which is connected to the voltage of a substrate by virtue of being in

electrical contact with P+ type channel stops which are in turn in electrical contact with the substrate.

Also in the charge transfer device art is the teaching of Janesick 5,077,592, which discloses an "open pinned-phase region" comprising a concentrated but very shallow implant of P-type dopant (B) in an n-channel 10, which connects the surface potential to the voltage of a substrate and acts as a virtual gate.

Would it be possible for one to make the element Applicant identifies as a "Pinned Transfer Gate" by following the teachings of Hynecek 4,994,875 or Janesick 5,077,592? In either of these two cases, Applicant should say so. If one skilled in the art could make the "Pinned Transfer Gate" and connect it to the voltage of a substrate by following some other teaching, Applicant should identify that teaching.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164

USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 of copending Application No.09/977,444 claims an imager cell including a substrate having a voltage, the imager cell comprising a photoreceptor; a sense node; and a pinned transfer gate comprising a p-doped pinned region in an n-doped transfer region connected to the voltage and further being configured to transfer charge between the photoreceptor and the sense node. Claim 1 of copending Application No.09/977,444 does not claim that the pinned transfer gate is disposed between the photoreceptor and the sense node. However, since claim 1 of copending Application No.09/977,444 claims that the pinned transfer gate is configured to transfer charge between the photoreceptor and the sense node, it is considered that one having skill in the art would have understood disposing the pinned transfer gate between the photoreceptor and the sense node to be the optimal location to accomplish this claimed function.

As obvious variants of claim 2 (per applicant's admission in Paper #8 filed on 4/29/03) claims 1, 3-34 and 58-71 are also rejected as obvious over claim 1 of copending Application No. 09/977,444. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1 and 5-8 are rejected under 35 U.S.C. 102(e) as being anticipated by GUIDASH (20020121656).

Guidash discloses an imager cell including a substrate 4 having a voltage, the imager cell comprising a photoreceptor, being a photodiode 12, a sense node 24; and a pinned transfer gate 14 disposed between the photoreceptor 12 and the sense node 24, the pinned transfer gate 14 being connected to the substrate 4 voltage and further being configured to transfer charge between the photoreceptor 12 and the sense node 24, a reset transistor 16 disposed to reset the sense node 12, and an output amplifier

18, being configured as a source follower amplifier, coupled to the sense node 24. Note figures 2 and 5 of Guidash.

B. Claims 1,2, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by the device depicted in figure 1 of ZHENG et al. (20020121655).

Zheng et al. discloses an imager cell including a substrate 20 having a voltage, the imager cell comprising a photoreceptor, being a photodiode 22, a sense node (the drain of the p-MOSFET), and a pinned transfer gate (the p-MOSFET) disposed between the photoreceptor 22 and the sense node, the pinned transfer gate being connected to the substrate 20 voltage and further being configured to transfer charge between the photoreceptor 22 and the sense node, wherein the pinned transfer gate comprises a p-doped pinned region (labeled p+) in an n-doped transfer region (labeled n-well). Note figure 1 of Zheng et al.

C. Claims 1,3,4, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by the device depicted in figure 5 of ZHENG et al. (20020121655).

Zheng et al. discloses an imager cell including a substrate 82 having a voltage, the imager cell comprising a photoreceptor, being a photogate, a sense node 96, and a pinned transfer gate 83 disposed between the photoreceptor and the sense node 96, the pinned transfer gate 83 being connected to the substrate 82 voltage and further being configured to transfer charge between the photoreceptor (photogate) and the sense node 96, and a photoreceptor readout gate 94 disposed above the photoreceptor (photogate). Note figure 5 of Zheng et al.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over ZHENG et al. (20020121655) in view of TURKO et al. (5,121,214).

Zheng et al. discloses an imager cell with all the limitations of claims 9-11, including a photoreceptor readout gate, except a readout clock connection coupled to the photoreceptor readout gate, control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock, the photoreceptor readout clock is characterized by a V+ level applied during an integration period, and a V- level applied during a transfer period. Note figure 5 of Zheng et al.

However, Turko et al. discloses an imaging array with a readout clock connection 18 coupled to a photoreceptor readout gate, control circuitry 14 coupled to the readout clock connection 18, the control circuitry 14 supplying a photoreceptor readout clock 68, the photoreceptor readout clock 68 is characterized by a V+ level (the upper value of clock trace 68) applied during an integration period 92, and a V- level (the lower value of clock trace 68) applied during a transfer period 94. Note figures 1 and 3 of Turko et al. Therefore, it would have been obvious to a person having skill in the art to

augment Zheng et al.'s imager cell with the readout clock connection coupled to a photoreceptor readout gate, control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock, the photoreceptor readout clock characterized by a V+ level applied during an integration period, and a V- level applied during a transfer period, such as taught by Turko et al. in order to compress the charge of an entire video field into a single video line to thus provide that the resultant line can then be "dumped" out of a horizontal register by sequencing the combined charges out past a charge coupled amplifier.

B. Claims 2-34 and 58-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over GUIDASH (20020121656).

Guidash discloses an imager cell including a substrate 4 having a voltage, the imager cell comprising a photoreceptor, being a photodiode 12, a sense node 24; and a pinned transfer gate 14 disposed between the photoreceptor 12 and the sense node 24, the pinned transfer gate 14 being connected to the substrate 4 voltage and further being configured to transfer charge between the photoreceptor 12 and the sense node 24. These elements are all the elements of claim 1. By applicant's express admission, claims 2-34 and 58-71 are obvious over these elements. See Paper #8 filed on 4/29/03, page 7.

C. Claims 2-34 and 58-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over the device depicted in figure 1 of ZHENG et al. (20020121655).

Zheng et al. discloses an imager cell including a substrate 20 having a voltage, the imager cell comprising a photoreceptor, being a photodiode 22, a sense node (the

drain of the p-MOSFET), and a pinned transfer gate (the p-MOSFET) disposed between the photoreceptor and the sense node, the pinned transfer gate being connected to the substrate 20 voltage and further being configured to transfer charge between the photoreceptor 22 and the sense node. Note figure 1 of Zheng et al. These elements are all the elements of claim 1. By applicant's express admission, claims 2-34 and 58-71 are obvious over these elements. See Paper #8 filed on 4/29/03, page 7.

D. Claims 2-34 and 58-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over the device depicted in figure 5 of ZHENG et al. (20020121655).

Zheng et al. discloses an imager cell including a substrate 82 having a voltage, the imager cell comprising a photoreceptor, being a photogate, a sense node 96, and a pinned transfer gate 83 disposed between the photoreceptor and the sense node 96, the pinned transfer gate 83 being connected to the substrate 82 voltage and further being configured to transfer charge between the photoreceptor (photogate) and the sense node 96. Note figure 5 of Zheng et al. These elements are all the elements of claim 1. By applicant's express admission, claims 2-34 and 58-71 are obvious over these elements. See Paper #8 filed on 4/29/03, page 7.

Response to Arguments

8. Applicant's arguments filed 10/16/03 have been fully considered but they are not persuasive.

It is argued, at page 17 of the remarks, that "As is known in the art, there are numerous ways for connecting a substrate, such as substrate 202, and a substrate region, such as p++ doped pinned region 219, to the same potential." However, the pinned transfer gate electrically connected to the substrate is a critical part of applicant's invention, in that it is only the substitution of the pinned transfer gate in applicant's claimed combination for the clocked transfer gate in the prior art, that distinguishes applicant's claims in any way from the prior art. The examiner takes the position that it is applicant's duty under § 112 to teach at least one way to make and use the pinned transfer gate, or else point to where such a way may be found in the prior art.

It is further argued, at page 17 of the remarks, that "pinned transfer gate 206 does not rely upon a conventional transistor gate structure..." However, applicant provides no hint as to the unconventional structure relied upon by the pinned transfer gate accomplishes the same results as the conventional transistor gate structure it replaces. Further, applicant has not claimed his unconventional gate structure in a way that avoids reading on the conventional structure.

It is argued, at pages 18-19 of the remarks, that "the pinned transfer gate [of claim 1 distinguishes from Guidash 2002/0121656 because it] is pinned to the same potential as the substrate, and, as such, does not require a conventional transistor gate structure to transfer charge, i.e., from the photoreceptor to the sense node." (emphasis added) However, in the first instance claim 1 requires a connection, not a pinning. In the second instance, it is not what the claimed

pinned transfer gate does not require, but rather, what it does require, that defines the scope of claim 1.

It is argued, at page 20 of the remarks, that "applicant reserves the right to provide declarations and/or documents under 37 CFR § 1.131 to "swear behind" the effective filing date of Zheng '655." However, applicant should remain aware that the 102(e) date (effective date) of a published U.S. application is the earliest U.S. filing date for which the published application properly seeks a benefit under 35 USC § 119(e), 35 USC § 120, or a combination of these sections. In the case of Zheng '655 that date is October 7, 1998.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. After February 4, 2004, this telephone number will change to (571) 272-1913. The examiner can normally be reached on Monday through Thursday 8 AM to 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

tld
12/2003

Minhloan Tran
Primary Examiner
Art Unit 2826